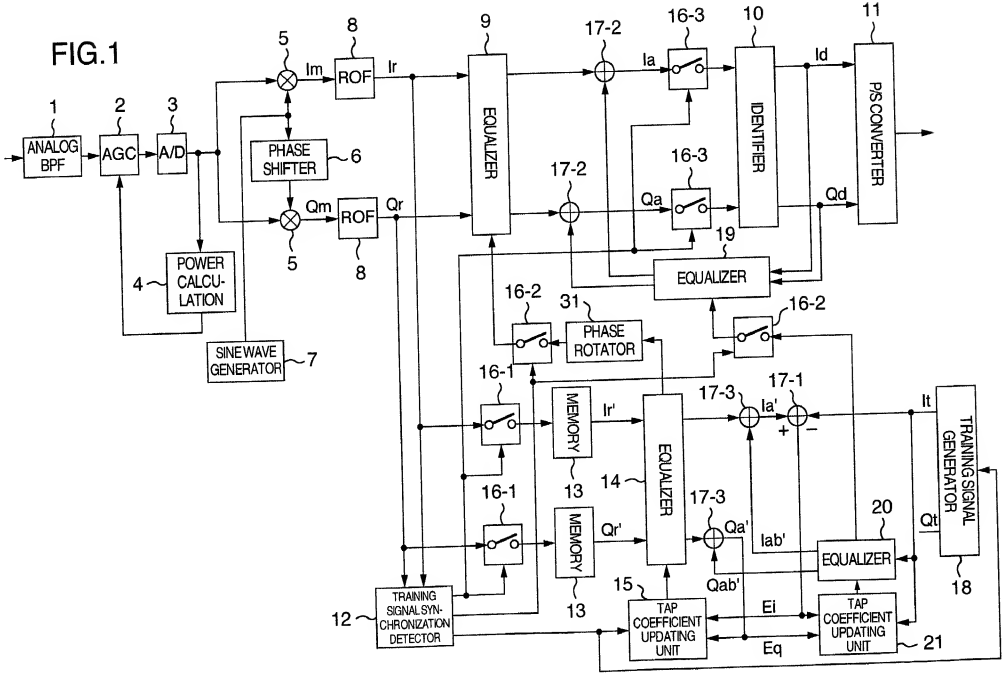
FUJITSU-E2CE2800

FIG.1



E 5732

FIG.2

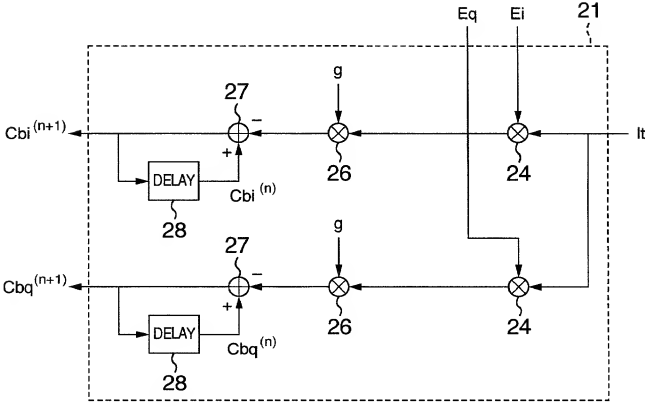

Eq
Ei
21
g
27
Cbi (n+1)
−
+
It
DELAY
Cbi (n)
26
24
28
g
27
Cbq (n+1)
−
+
DELAY
Cbq (n)
26
24
28

FIG.3

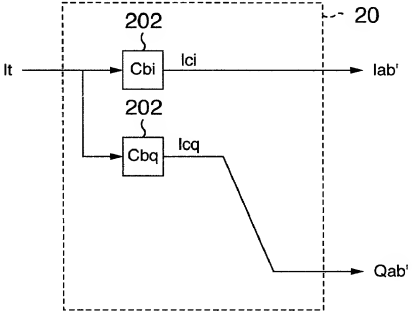

20
202
It
Cbi
Ici
Iab'
202
Cbq
Icq
Qab'

FIG.4

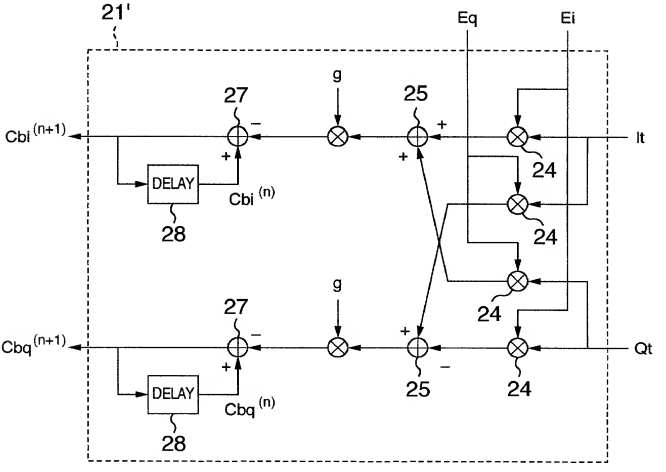

21'
Eq
Ei
g
27
25
Cbi (n+1)
It
DELAY
Cbi (n)
28
24
24
24
g
27
Cbq (n+1)
Qt
DELAY
Cbq (n)
28
25
24

FIG.5

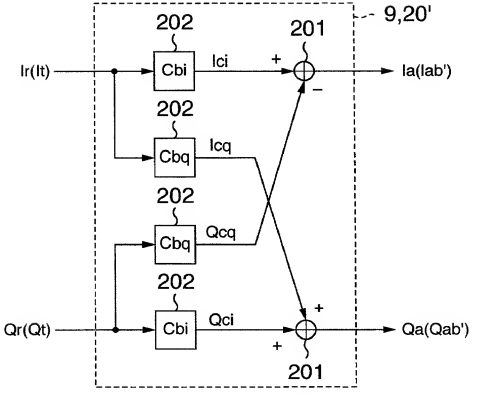

9,20'
202
201
Cbi
Ici
+
−
Ir(It)
Ia(Iab')
202
Cbq
Icq
202
Cbq
Qcq
202
Cbi
Qci
+
+
Qr(Qt)
Qa(Qab')
201

FIG.6

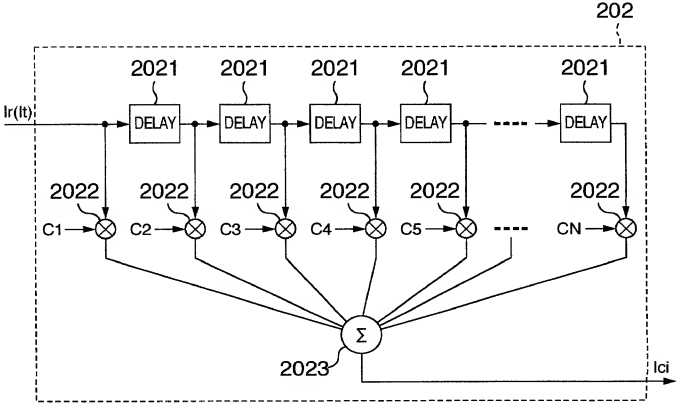

202
2021
2021
2021
2021
2021
Ir(It)
DELAY
DELAY
DELAY
DELAY
DELAY
2022
2022
2022
2022
2022
2022
C1
C2
C3
C4
C5
CN
Σ
2023
Ici

FIG.7

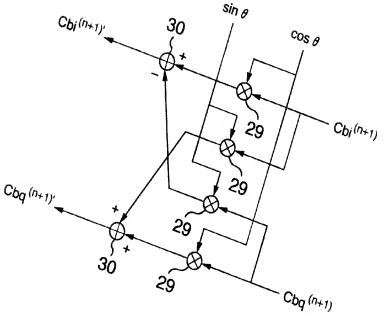

Cbi (n+1)'
30
sin θ
cos θ
29
Cbi (n+1)
Cbq (n+1)'
29
29
30
29
Cbq (n+1)

FIG.8

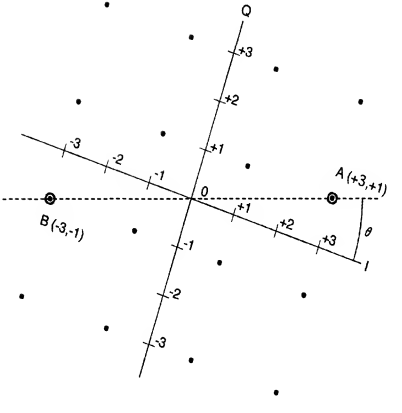
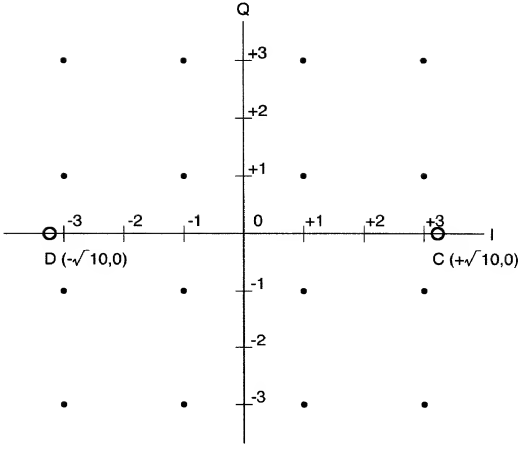
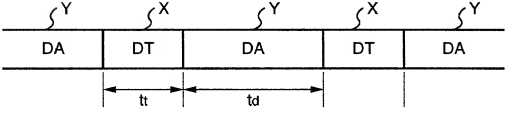

Q
+3
+2
+1
-3
-2
-1
0
+1
+2
+3
A (+3,+1)
B (-3,-1)
θ
I
-1
-2
-3

FIG.9



O SIGNAL POINT OF TRAINING SIGNAL

FIG.10



EUROPEAN PATENT APPLICATION

FIG.11
PRIOR ART

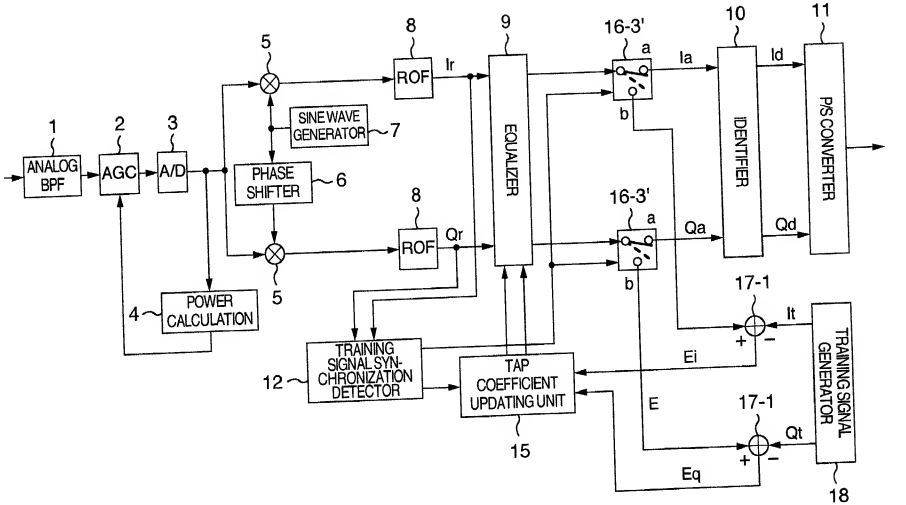
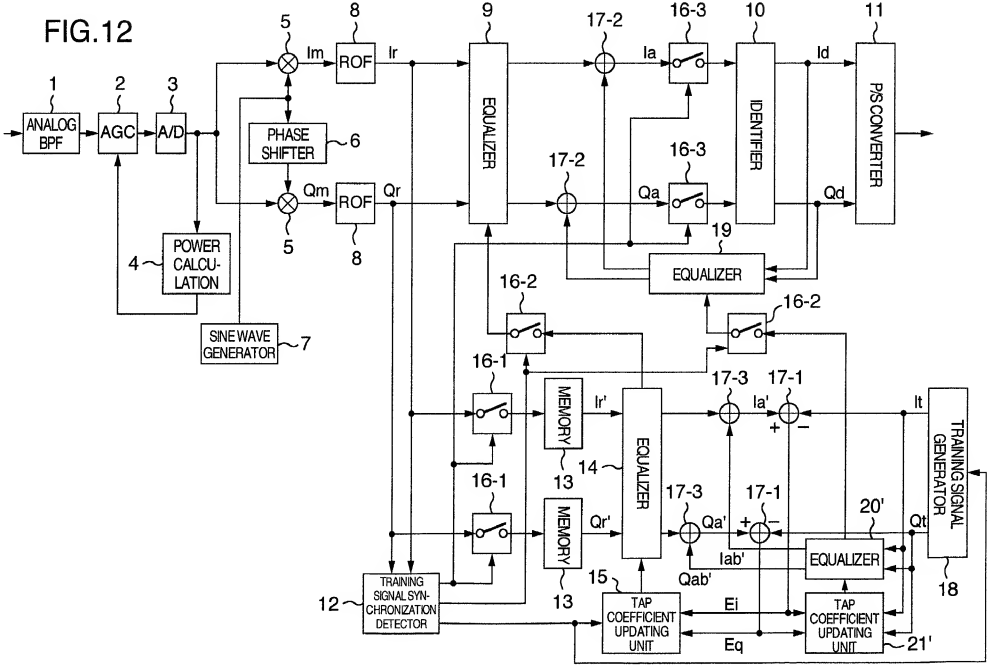


FIG.12


1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
Qm
5
PHASE SHIFTER
6
SINE WAVE GENERATOR
7
8
ROF
Ir
8
ROF
Qr
9
EQUALIZER
17-2
Ia
17-2
Qa
16-3
16-3
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
19
EQUALIZER
16-2
16-2
16-1
16-1
MEMORY
Ir'
MEMORY
Qr'
13
13
14
EQUALIZER
17-3
Ia'
17-1
17-3
Qa'
17-1
Iab'
Qab'
20'
EQUALIZER
It
Qt
TRAINING SIGNAL GENERATOR
18
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
TAP COEFFICIENT UPDATING UNIT
21'

PUBLISHED BEFORE

FIG.13

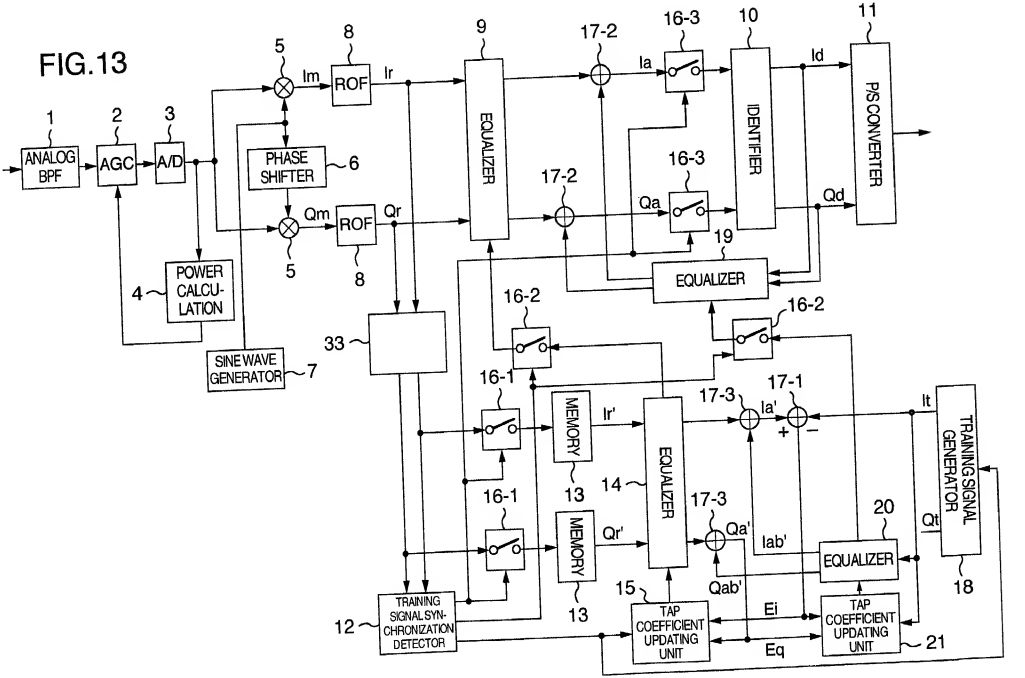
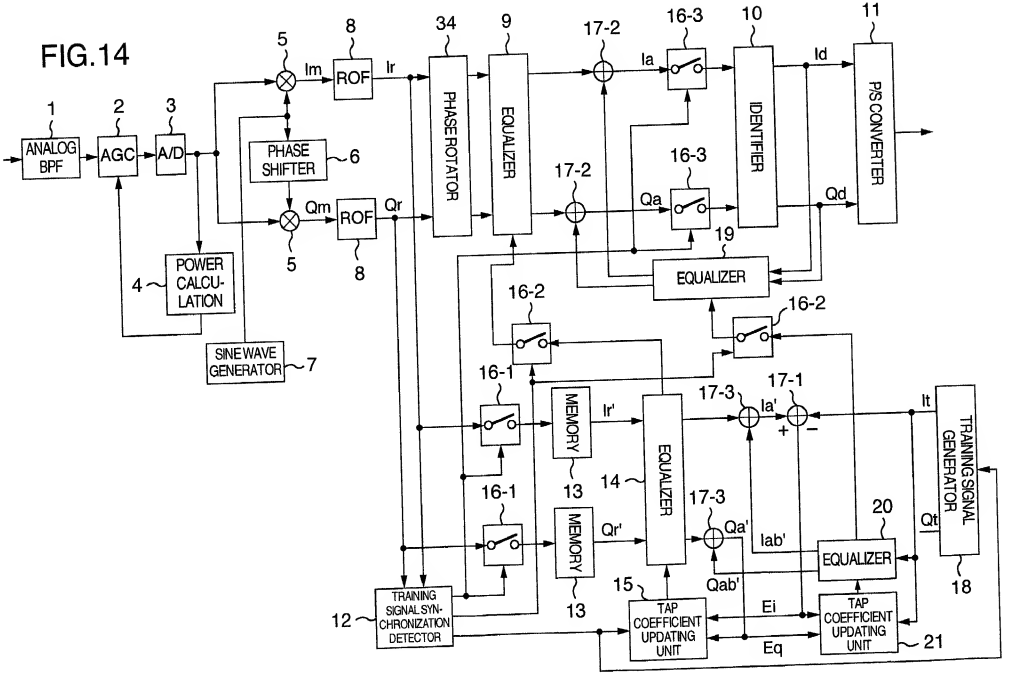


FIG.14


1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
Qm
ROF
8
Ir
Qr
PHASE SHIFTER
6
SINE WAVE GENERATOR
7
34
PHASE ROTATOR
9
EQUALIZER
17-2
Ia
Qa
16-3
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
19
EQUALIZER
16-2
16-1
MEMORY
Ir'
Qr'
13
14
EQUALIZER
17-3
Ia'
17-1
It
+
−
16-1
MEMORY
13
17-3
Qa'
Iab'
20
EQUALIZER
Qt
TRAINING SIGNAL GENERATOR
18
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
15
Qab'
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
TAP COEFFICIENT UPDATING UNIT
21

FOUND ACCESSED

FIG.15

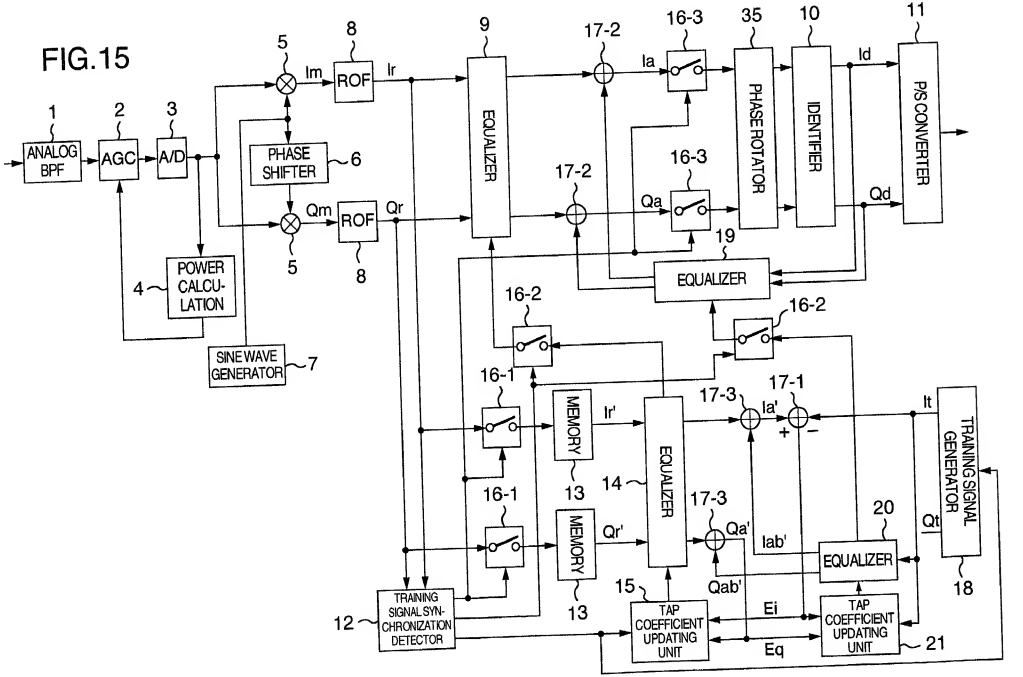


FIG.16

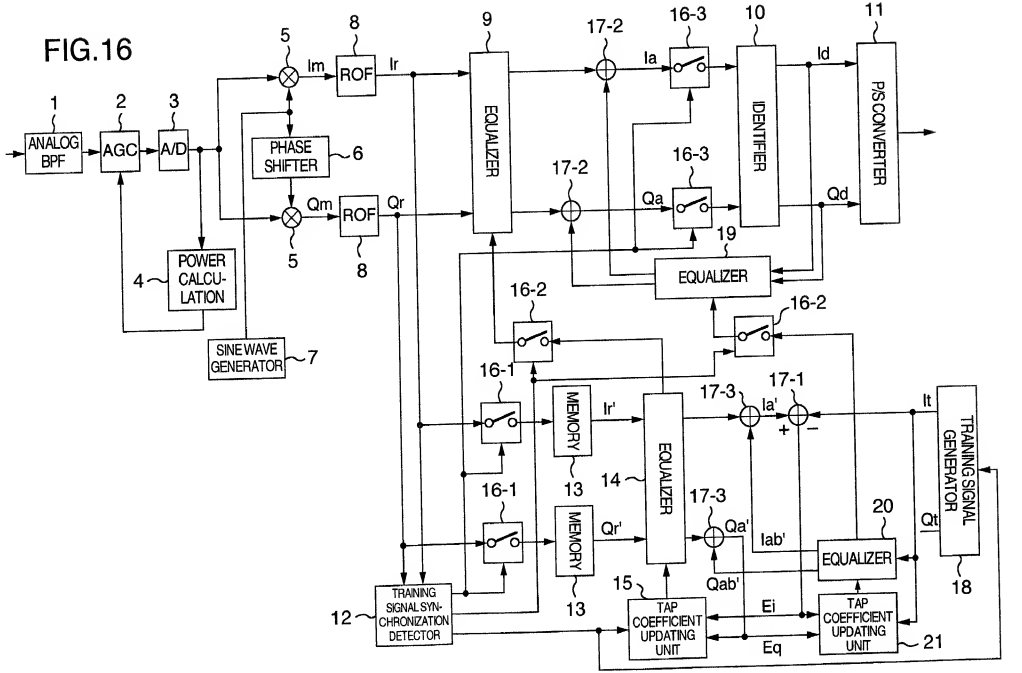

1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
Qm
PHASE SHIFTER
6
SINE WAVE GENERATOR
7
8
ROF
Ir
Qr
9
EQUALIZER
17-2
Ia
Qa
16-3
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
19
EQUALIZER
16-2
16-1
MEMORY
Ir'
Qr'
13
14
EQUALIZER
17-3
Ia'
17-1
It
TRAINING SIGNAL GENERATOR
18
Qa'
Iab'
20
EQUALIZER
Qt
Qab'
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
21
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR

FIG.17

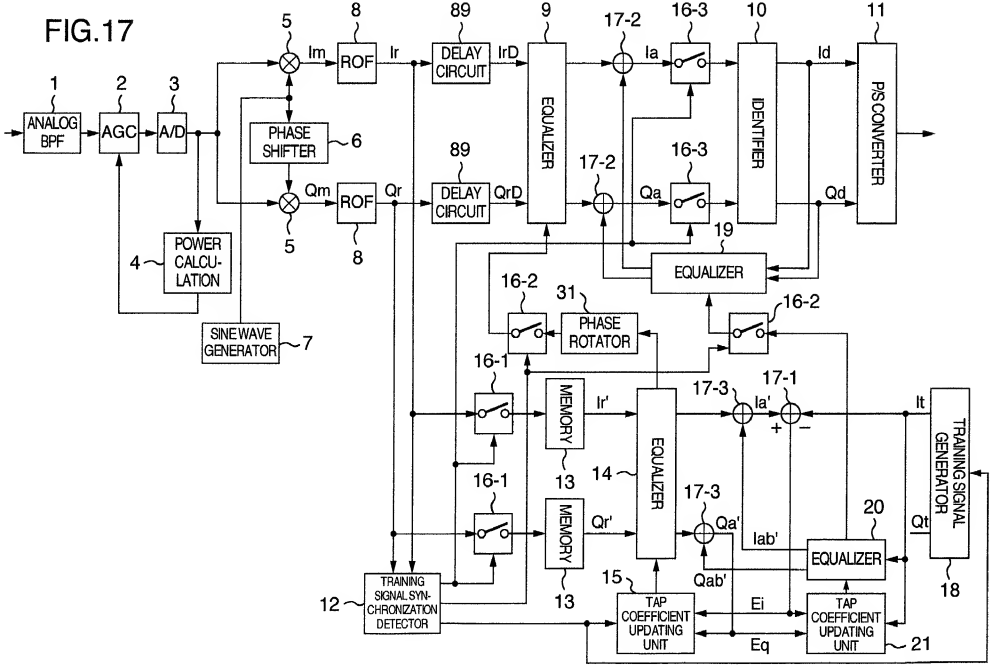

1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
Qm
5
PHASE SHIFTER
6
SINE WAVE GENERATOR
7
8
ROF
Ir
8
ROF
Qr
89
DELAY CIRCUIT
IrD
89
DELAY CIRCUIT
QrD
9
EQUALIZER
17-2
Ia
17-2
Qa
16-3
16-3
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
19
EQUALIZER
16-2
31
PHASE ROTATOR
16-2
16-1
16-1
MEMORY
Ir'
MEMORY
Qr'
13
13
14
EQUALIZER
17-3
Ia'
17-1
+
−
17-3
Qa'
Iab'
It
20
EQUALIZER
Qt
TRAINING SIGNAL GENERATOR
18
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
TAP COEFFICIENT UPDATING UNIT
21
Qab'

FIG.18

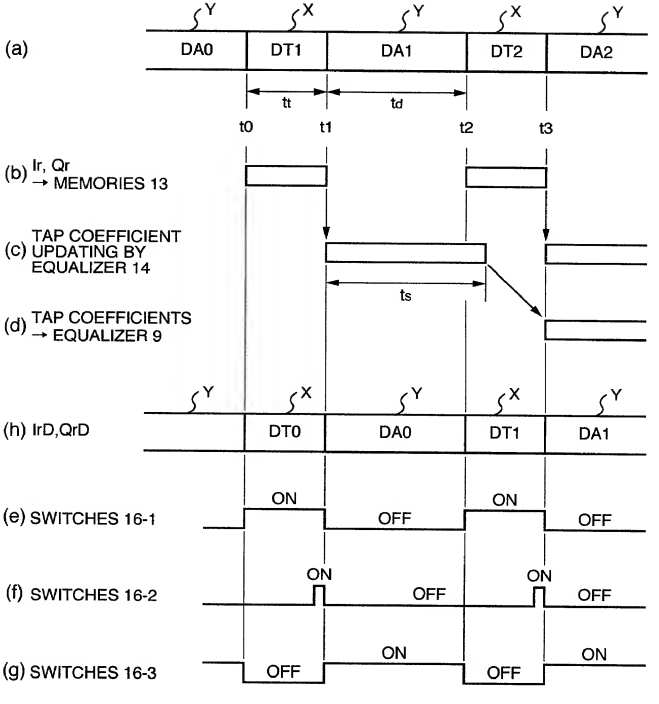

(a)
Y
X
Y
X
Y
DA0
DT1
DA1
DT2
DA2
tt
td
t0
t1
t2
t3
(b) Ir, Qr → MEMORIES 13
(c) TAP COEFFICIENT UPDATING BY EQUALIZER 14
ts
(d) TAP COEFFICIENTS → EQUALIZER 9
(h) IrD,QrD
DT0
DA0
DT1
DA1
(e) SWITCHES 16-1
(f) SWITCHES 16-2
(g) SWITCHES 16-3
ON
OFF

FIG.19

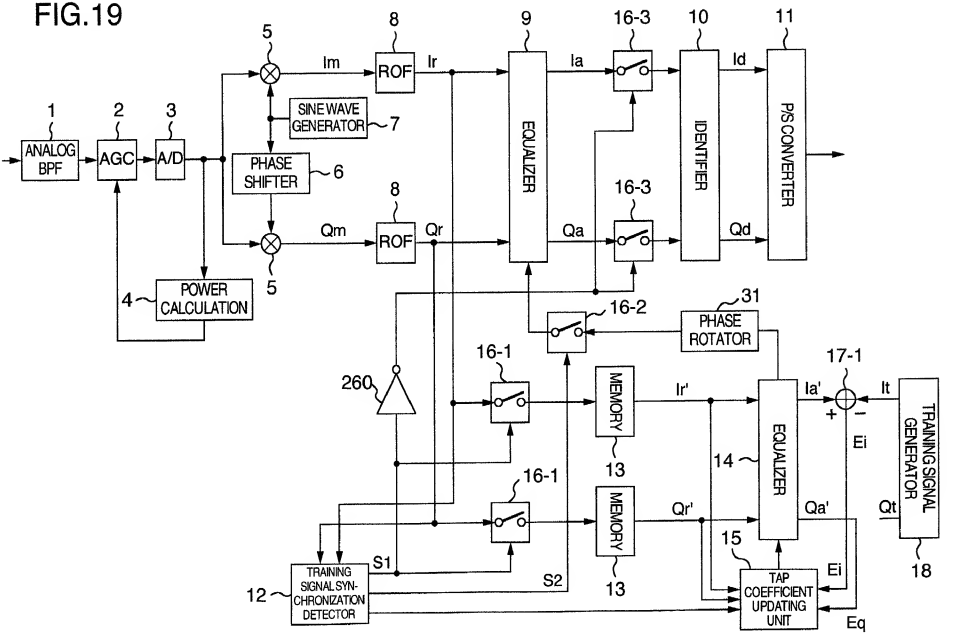

1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCULATION
5
5
Im
Qm
SINE WAVE GENERATOR
7
PHASE SHIFTER
6
8
ROF
Ir
8
ROF
Qr
9
EQUALIZER
Ia
Qa
16-3
16-3
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
16-2
31
PHASE ROTATOR
16-1
16-1
260
MEMORY
13
MEMORY
13
Ir'
Qr'
14
EQUALIZER
Ia'
Qa'
17-1
+
−
It
Ei
Qt
TRAINING SIGNAL GENERATOR
18
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
S1
S2

FIG.20

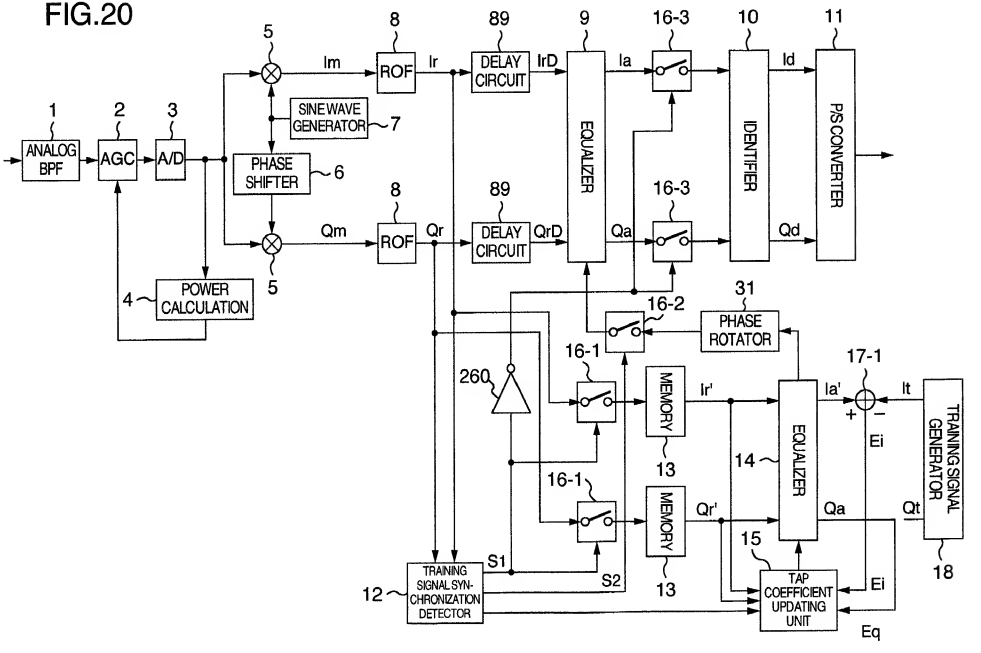
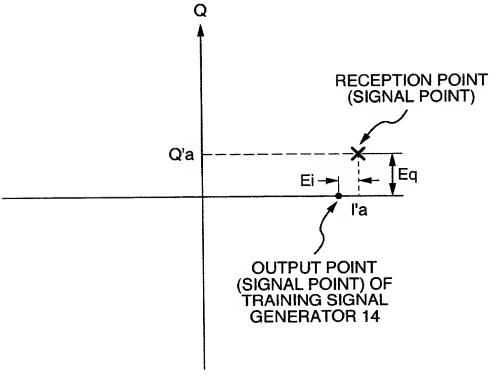

1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCULATION
5
5
Im
Qm
SINE WAVE GENERATOR
7
PHASE SHIFTER
6
8
ROF
Ir
8
ROF
Qr
89
DELAY CIRCUIT
IrD
89
DELAY CIRCUIT
QrD
9
EQUALIZER
16-3
Ia
16-3
Qa
10
IDENTIFIER
Id
Qd
11
P/S CONVERTER
31
PHASE ROTATOR
16-2
16-1
260
16-1
MEMORY
Ir'
13
MEMORY
Qr'
13
14
EQUALIZER
Ia'
Qa
17-1
+
−
Ei
It
Qt
TRAINING SIGNAL GENERATOR
18
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
12
TRAINING SIGNAL SYNCHRONIZATION DETECTOR
S1
S2

FIG.21


Q
RECEPTION POINT
(SIGNAL POINT)
Q'a
Ei
Eq
I'a
OUTPUT POINT
(SIGNAL POINT) OF
TRAINING SIGNAL
GENERATOR 14